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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,207	04/02/2004	Kenneth S. Gockjian	A2004003	2438

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EXAMINER	
UNELUS, ERNEST	
ART UNIT	**PAPER NUMBER**
2181	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/817,207	GOEKJIAN ET AL.	
	Examiner	Art Unit	
	Ernest Unelus	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO AMENDMENT

Claim rejections based on prior art

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/12/07 has been entered.

The instant application having Application No. 10/817,207 has a total of 3 preliminary amended claims pending in the application; there is 1 independent claim and 2 dependent claims, all of which are ready for examination by the examiner.

Applicant's arguments filed 04/12/2007, with respect to the rejection(s) of claim(s) 1-3 under Kabenjian (US pat. 5,613,162) have been fully considered and is not persuasive.

The applicant argues that Kabenjian, the cited reference, does not teach that the DMA controller loads the stored parameters that enable the data access between the port and the memory.

This argument is found to be persuasive because col. 10, lines 40-61, discloses through a command from the CPU, the registers that are inside the DMA are set with parameters. See fig. 4, as an example of the register block. As discloses in col. 13, lines 15-

17, "Thus, the values in the I/O parameter registers are selected to adapt the timing of the DMA transfers to the data transfer characteristics of the I/O device". The *loading* of the parameters, as discloses in the claim language, is being interpreted by the examiner as the parameters being selected. See fig. 9C and col. 17, lines 6-39 for more detail, witch discloses a port having access to the memory).

In regards to the FIFOs "located at and is dedicated to", as the applicant discloses in the remarks, see col. 8, lines 45-60, which discloses, "The DMA unit 200 of the preferred embodiment has four independent DMA channels. A first DMA channel comprises the first register block 300 and the first data buffer 252. A second DMA channel comprises the second register block 320 and the second data buffer 254. A third DMA channel comprises the third register block 340 and the third data buffer 256. A fourth DMA channel comprises the fourth register block 360 and the fourth data buffer 258. Each DMA channel in the DMA unit 200 is preferably used for DMA transfers with a particular I/O device or a particular group of I/O devices. For example, the first DMA channel may be used with the IDE controller 154, the second DMA channel may be used with the graphics controller 160, the third DMA channel may be used with the SCSI controller 162, and the fourth DMA channel may be used with the LAN controller 166". Col. 18, lines 9-15 also discloses "The present invention is also advantageous because it permits multiple DMA devices to share the same bus. By using independent control registers and data buffers, and by releasing the data bus after the data from or to each buffer is transferred, the present invention permits the data transfers from different DMA devices to be interleaved"

The applicant has cancelled claims 4-6.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

4. As required by **M.P.E.P. 609(C)**, the applicant's previously submissions of the Information Disclosure Statement dated August 11, 2006 has previously been acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner has been attached to a previous office action

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. **Claims 1-3** are rejected under 35 U.S.C. 102(b) as being anticipated by Kabenjian (US pat. 5,613,162).

7. As per **claim 1**, Kabenjian discloses "a context based direct memory access architecture **(computer system 90 of fig. 1)**, comprising:

a memory **(memory 120 of fig. 1)**;

a plurality of ports **(the four I/O access points of the multiple devices, such as controller 154, 160, 162, and 166 in fig. 1. These access points are the DMA channels discloses in col. 8, lines 45-60)**, wherein each port has an associated buffer located at and dedicated to the port for temporarily storing data transferred through the port, and wherein each port has an associated direct memory access channel for accessing the memory **(see col. 8, lines 45-60, which discloses, "The DMA unit 200 of the preferred embodiment has four independent DMA channels. A first DMA channel comprises the first register block 300 and the first data buffer 252. A second DMA channel comprises the second register block 320 and the second data buffer 254. A third DMA channel comprises the third register block 340 and the third data buffer 256. A fourth DMA channel comprises the fourth register block 360 and the fourth data buffer 258. Each DMA channel in the DMA unit 200 is preferably used for DMA transfers with a particular I/O device or a particular group of I/O devices. For example, the first DMA channel may be used with the IDE controller 154, the second DMA channel may be used with the graphics controller 160, the third DMA channel may be used with the SCSI controller 162, and the fourth DMA channel may be**

used with the LAN controller 166". See also col. 9, lines 49-55, which discloses transfer between the memory and the controllers through the DAM unit);

a direct memory access controller **(DMA controller 202 in fig. 1)** that receives requests for accessing the memory by the plurality of ports **(see col. 17, lines 6-22, which gives an example of IDE controller 154 getting access of the memory through buffer 252, which is part of that the IDE controller's port, as explained above. Note; buffer 252 is associate with the DMA controller 202, as discloses in col. 8, lines 45-60. See also col. 7, lines 15-36, which discloses that access to the memory by any of the devices is made though a request),** wherein each request is received from one of the plurality of ports **(see col. 7, lines 15-36 and col. 8, lines 45-60)**, and wherein the direct memory access controller stores parameters **(the values in the parameter register, such as register block 1, as discloses in col. 13, line 15. see fig. 4)** defining the direct memory access operations for each port **(see fig. 4 and col. 13, lines 10-17, which discloses "In the preferred embodiment, the I/O device parameter registers are loaded by the system basic input/output system (BIOS) during system initialization because at that time it will be known which I/O devices are present and which DMA channels are dedicated to particular I/O resources. Thus, the values in the I/O parameter registers are selected to adapt the timing of the DMA transfers to the data transfer characteristics of the I/O device")**, and wherein after a request is received from a port the direct memory access controller loads the parameters for the current direct memory access operation responsive to the request from the port to enable the port to access the memory and transfer data between the memory and the buffer associated with the port **(see col. 7, lines 15-35, which discloses that a device, such a controller, begin a transfer to the memory by first sending a**

request to win access on the bus 152 through the arbiter; as lines 15-17 discloses "When a device, such as the CPU 100, needs to access another device in the computer system 90, the first device must first request control of the buses required to complete the access". As a response of wining access on the bus, the values in the parameter register is selected, as discloses in col. 13, lines 15-17, "Thus, the values in the I/O parameter registers are selected to adapt the timing of the DMA transfers to the data transfer characteristics of the I/O device". The *loading* of the parameters, as discloses in the claim language, is being interpreted by the examiner as the parameters being selected. See fig. 9C and col. 17, lines 6-39 for more detail, witch discloses a port having access to the memory).

8. As per **claim 2**, Kabenjian further discloses comprising a central parameter store **(register block 1 of fig. 4)** for storing parameters for each of a plurality of DMA channels corresponding to each of the plurality of ports **(see col. 13, lines 5-17)**.

9. As per **claim 3**, Kabenjian discloses wherein the direct memory access controller further comprises means for servicing the request **(see fig. 4 and col. 3, lines 20-52. Col. 11, lines 29-31 also discloses "The DMA controller 202 keeps track of each DMA transfer requested to ensure that each DMA transfer is completed")**, comprising: means **(data buffer 252 of fig. 3)** for queuing a memory operation **(see col. 17, lines 26-30)**; means **(DMA controller 202 of fig. 2)** for updating parameters **(see Col. 12, line 63 to col. 13, line 17)**; and means **(register block 1 of fig. 4)** for fetching and storing parameters in the central parameter store **(see fig. 4 and col. 3, lines 20-52).**

RELEVANT ART CITED BY THE EXAMINER

10. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See MPEP 707.05(c).

11. The following references teach an apparatus for communicating data among devices interconnected by a shared a shared access memory.

U.S. PATENT NUMBER

US 5,978,866

US 2004/0177225

US 6,795,875

CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

12. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

13. Per the instant office action, claims 1-3 have received a first action on the merits and are subject of a first action non-final.

DIRECTION OF FUTURE CORRESPONDENCES

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ernest Unelus whose telephone number is (571) 272-8596. The examiner can normally be reached on Monday to Friday 9:00 AM to 5:00 PM.

IMPORTANT NOTE

15. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Alford Kindred, can be reached at the following telephone number: Area Code (571) 272-4037.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PMR system, see her//pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217- 91 97 (toll-free).

June 27, 2007

Ernest Unelus
Patent Examiner
Art Unit 2181

ALFORD KINDRED
PRIMARY EXAMINER